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KAMALA INSTITUTE OF TECHNOLOGY & SCIENCE, SINGAPUR**23EC28PC404****II.B. Tech. II. Semester Regular/Supplementary Examinations, April/May- 2026****LINEAR & DIGITAL IC APPLICATIONS****(ECE)****Time: 3 Hours****Max. Marks: 60**

Note: Question paper consists of Part-A & Part-B.

i) **Part-A** for 10M, ii) **Part-B** for 50marks

- Part A** is compulsory, consisting of 10 sub questions from all units carrying equal marks.
- Part-B** consists of **10 questions** (numbered from 2 to 11) carrying **10marks** each. From each unit there are 2 questions and the students should answer one of them. Hence the student should answer **5 questions** from **Part-B**.

PART-A (10Marks)			
Q. No	Questions	Marks	BTL
1.a)	Mention the reasons why open loop Op-Amp is not preferred for linear applications.	1M	1
1.b)	How comparator circuit is used as zero crossing detector.	1M	1
1.c)	Draw the circuit diagram of All pass filter?	1M	1
1.d)	Discuss the applications of a 555 timer operating in astable multivibrator mode.	1M	2
1.e)	Define resolution in ADC?	1M	1
1.f)	What is disadvantage of weighted resistor DAC?	1M	1
1.g)	Describe the function of an encoder.	1M	2
1.h)	Distinguish between decoder and demultiplexer?	1M	2
1.i)	List the advantages of synchronous counter over asynchronous counter?	1M	1
1.j)	Describe the various applications of ROMs in digital systems.	1M	2
PART-B (50Marks)			
Q.No	Questions	Marks	BTL
2. a)	Construct the closed loop inverting amplifier circuit and derive the voltage gain.	5M	3
b)	Design a differentiator circuit that will differentiate input signal with $f_{max} = 100\text{Hz}$.	5M	3
OR			
3. a)	Construct the ideal integrator circuit and explain its drawbacks.	5M	2
b)	Design a Schmitt trigger circuit using op-amp with $V_{ut} = 4\text{V}$, $V_{Lt} = -2\text{V}$ and output voltage swing $= \pm 10\text{V}$.	5M	3
OR			
4. a)	Design an astable multivibrator using 555 with a frequency of 1KHz for the duty cycles of 60%?	5M	3
b)	With a neat diagram explain about triangular wave generator and derive the frequency of oscillation.	5M	2
OR			

5. a)	Describe the operation of IC555 timer in monostable mode.	5M	3
b)	Explain the principle of PLL with neat block diagram?	5M	2
6. a)	Demonstrate the Dual-Slope ADC with a neat block diagram and explain its working principle.	6M	3
b)	Determine the output voltage of DAC for the following digital inputs with full scale voltage of 5V. 1. 10 (2bit DAC) 2. 1010(4bit DAC) 3. 10111010 (8bit DAC)	4M	4
OR			
7. a)	Illustrate 3-bit R-2R ladder type DAC with neat circuit diagram.	5M	2
b)	Compare Parallel type, successive Approximation type ADC and Dual slope ADC.	5M	3
8. a)	Design a 4 X 16 decoder using 74138 IC.	5M	3
b)	Design a 4-bit parallel adder/subtractor circuit using IC7483 and suitable logic gates.	5M	3
OR			
9. a)	Implement the logic function $F(A,B,C) = \sum(1,2,4,6,7)$ using IC74151	5M	4
b)	Analyze the working of a priority encoder with truth table and logic diagram.	5M	3
10.a)	Compare the differences between SRAM and DRAM.	5M	3
b)	Design a MOD-100 counter using IC7490 and draw the circuit diagram.	5M	3
OR			
11.a)	Design a shift register circuit using a D-flip flop (IC7474).	5M	3
b)	Describe the internal architecture of ROM (that stores 4K bytes and uses a square register array).	5M	3