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KAMALA INSTITUTE OF TECHNOLOGY & SCIENCE, SINGAPUR
23EC28ES404

II B. Tech. II. Semester Regular/Supplementary Examinations, April/May- 2026
DIGITAL ELECTRONICS
(EEE)

Time: 3 Hours

Max. Marks: 60

Note: Question paper consists of Part-A & Part-B.

i) **Part-A** for 10M, ii) **Part-B** for 50marks

- Part A** is compulsory, consisting of 10 sub questions from all units carrying equal marks.
- Part-B** consists of **10 questions** (numbered from 2 to 11) carrying **10marks** each. From each unit there are 2 questions and the students should answer one of them. Hence the student should answer **5 questions** from **Part-B**.

PART-A (10Marks)			
Q. No	Questions	Marks	BTL
1.a)	Write the Boolean expression for AND, OR gate.	1M	1
1.b)	Convert decimal 10 to binary.	1M	2
1.c)	Compare SOP and POS.	1M	1
1.d)	Why are don't cares used?	1M	2
1.e)	Define Half Adder and Full Adder.	1M	1
1.f)	How many select lines are needed for 8:1 MUX?	1M	2
1.g)	What is race around condition?	1M	1
1.h)	Name types of shift registers.	1M	1
1.i)	Define memory organization.	1M	1
1.j)	State different types of RAM.	1M	1
PART-B (50Marks)			
Q.No	Questions	Marks	BTL
2. a)	Explain the various logic gates with examples.	5M	4
b)	Simplify the following Boolean expressions by manipulation of Boolean algebra. $F(A, B, C, D) = A' C (A' B D)' + A' B C' D' + A B' C$	5M	3
OR			
3. a)	Convert the following to Decimal and then to Binary. i) $(3214)_{16}$ ii) $(2716)_8$	5M	3
b)	Given 2 binary numbers $X=1010100_{(2)}$ and $Y=1000011_{(2)}$. Perform 2's complement subtraction for $X-Y$ and $Y-X$.	5M	3
4.	Simplify the following Boolean functions, using a four variable Karnaugh map method and implement the simplified function using NAND gates. $F(A, B, C, D) = \Sigma (0, 2, 4, 5, 6, 7, 8, 10, 13, 15)$	10M	5
OR			
5.	Simplify the function in SOP and POS using K-Map $F(A, B, C, D) = \Sigma m(0, 1, 3, 4, 5, 9, 11, 12, 13, 15)$	10M	6

6.	Design a 4 bit adder-subtractor and explain its operation.	10M	6
OR			
7.	Design BCD to Excess-3 code converter and draw the logic diagram.	10M	6
8. a)	Explain the operation of clocked SR Flip flop with its characteristic table.	5M	4
b)	Distinguish between Sequential and combinational circuits.	5M	2
OR			
9.	Using D flip-flop, design a synchronous counter which counts in the sequence 000,001,010,011,100,101,110,111,000	10M	6
10.a)	Explain the operation of 16-bit ROM array with neat diagram.	5M	4
b)	Draw the basic circuit diagram of static RAM and explain its operation.	5M	4
OR			
11.a)	Briefly, explain about the programmable logic devices.	5M	4
b)	Explain the detailed logic configurable Block Architecture of FPGA.	5M	4

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